



40G QSFP+ Passive Cable

APCP04-QQCxxx-yy



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QSFP+ Passive Direct Attach Copper Cable assemblies were developed for high-density applications, offering a cost-effective, low-power option for high-speed data center interconnects. The QSFP+ form factor can replace up to four standard SFP+ connections, providing greater density and reduced system cost.

The direct-attach assemblies support emerging 40Gb/s applications and are available in standard lengths up to 7 meters with longer custom lengths available

Product Features

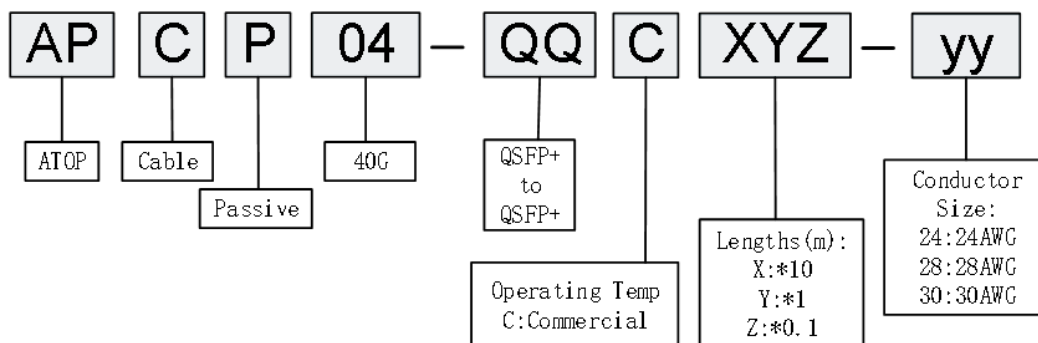
- ✓ Compliant with SFF-8436
- ✓ Fully compatible with IEEE802.3ba and InfiniBand QDR specifications
- ✓ 40 Gb/s total bandwidth
- ✓ 4 independent duplex channels operating at 10Gbps, also support for 2.5Gbps, 5Gbps data rates
- ✓ Low power, low latency analog circuitry
- ✓ Uses advanced analog signal processing technology
- ✓ All-metal housing for superior EMI performance
- ✓ BER better than 10⁻¹²
- ✓ Ultralow crosstalk for improved performance
- ✓ EEPROM for cable signature & system communications
- ✓ 30 AWG to 24AWG cable sizes available
- ✓ Tested in an end-to-end system
- ✓ RoHS compliant

Applications

- ✓ Data Server
- ✓ Networked storage systems
- ✓ Router
- ✓ External storage system
- ✓ Data Center networking
- ✓ Communications Switches
- ✓ Routers
- ✓ 40Gigabit Ethernet (40G BASE – Cr4)



Product Selection



Part Number	Lengths	Conductor Size	Note
APCP04-QQC005-yy	0.5m	26/28/30 AWG	1
APCP04-QQC010-yy	1m	26/28/30 AWG	1
APCP04-QQC015-yy	1.5m	26/28/30 AWG	1
APCP04-QQC020-yy	2m	26/28/30 AWG	1
APCP04-QQC025-yy	2.5m	26/28/30 AWG	1
APCP04-QQC030-yy	3m	26/28/30 AWG	1
APCP04-QQC050-yy	5m	26/28/30 AWG	1
APCP04-QQC070-yy	7m	26/28/30 AWG	1
APCP04-QQC100-yy	10m	26/28/30 AWG	1

Note:

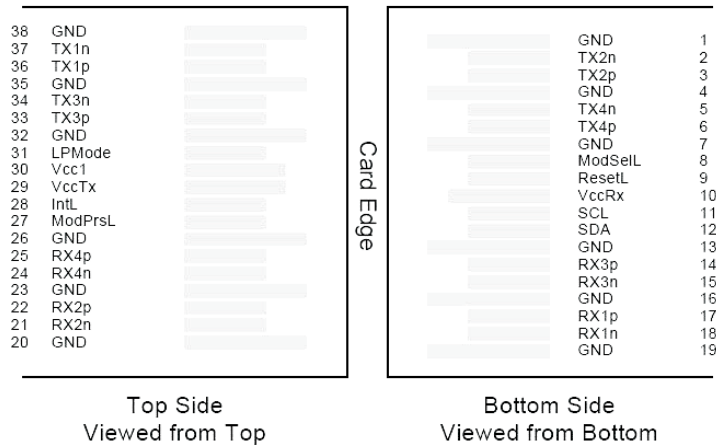
1, yy=30,28,26, present wire size AWG

Pin Descriptions

QSFP+ End

Pin	Symbol	Name	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	<p>The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module</p>	
9	ResetL	<p>The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.</p>	
10	VccRx	+ 3.3V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	

12	SDA	2-Wire Serial Interface Data
13	GND	GND
14	Rx3p	Receiver Non-Inverted Data Output, CML-O
15	Rx3n	Receiver Inverted Data Output, CML-O
16	GND	GND
17	Rx1p	Receiver Non-Inverted Data Output, CML-O
18	Rx1n	Receiver Inverted Data Output, CML-O
19	GND	Ground
20	GND	Ground
21	Rx2n	Receiver Inverted Data Output, CML-O
22	Rx2p	Receiver Non-Inverted Data Output, CML-O
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output, CML-O
25	Rx4p	Receiver Non-Inverted Data Output, CML-O
26	GND	Ground
27	ModPrsL	Module Present, connect to GND
28	IntL	The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.
29	VccTx	+3.3 V Power Supply transmitter
30	Vcc1	+3.3 V Power Supply
31	LPMoDe	The LPMoDe pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMoDe pin and the combination of the Power_over-ride and Power_set softwarecontrol bits (Address A0h, byte 93 bits 0,1).
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input, CML-I
34	Tx3n	Transmitter Inverted Data Output, CML-I
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input, CML-I
37	Tx1n	Transmitter Inverted Data Output, CML-I
38	GND	Ground



Pin-out of Connector Block on Host Board

Signal Integrity

ITEM	REQUIREMENT	TEST CONDITION				
Cable Impedance	105+5/-5Ω					
Differential Impedance	Paddle Card Impedance 100±10Ω	Rise time of 35ps (20% - 80%).				
Cable Termination Impedance	100±15Ω					
[Differential (Input/Output) Return loss SDD11/SDD22]	$\text{Return loss}(f) \geq \begin{cases} 10 & 0.01 \leq f < 4.1 \\ 6.3 - 13 \log_{10}(f/5.5) & 4.1 \leq f \leq 11.1 \end{cases}$ <p>Where f is the frequency in GHz Return loss(f) is the return loss at frequency f</p>	0.01GHz ≤ f ≤ 11.1GHz SFF-8431 Rev.4.1				
Differential Insertion Loss (SDD21 Max.)	(Differential Insertion Loss Max.)				10MHz ≤ f ≤ 11.1GHz	
	AWG \ F	600MHz	1.25GHz	2.5GHz		5.0GHz
	30(1m)Max	≥ -3.0dB	≥ -4.0dB	≥ -5.5dB		≥ -8.0dB
	30(2m)Max	≥ -5.0dB	≥ -6.5dB	≥ -9.5dB		≥ -14.0dB
	30(3m)Max	≥ -6.0dB	≥ -8.0dB	≥ -11.0dB		≥ -16.0dB
26(5m)Max	≥ -8.0dB	≥ -11.5dB	≥ -17.0dB	≥ -26.5dB		
24(10m)Max	≥ -3.0dB	≥ -4.0dB	≥ -5.5dB	≥ -8.0dB		
MDNEXT(multiple disturber near-end crosstalk)	≥ 26dB @ 5GHz				10MHz ≤ f ≤ 5GHz	
Insertion Loss Deviation	-0.7-0.2*10 ⁻³ f ≤ ILD ≤ 0.7+0.2*10 ⁻³ f (f is the frequency in MHz)				10MHz ≤ f ≤ 5GHz	

Other Electrical Performance

ITEM	REQUIREMENT	TEST CONDITION
Low Level Contact Resistance	80milliohms Max. From initial.	EIA-364-23:Apply a maximum voltage of 20mV And a current of 100 mA.
Insulation Resistance	10Mohm(Min.)	EIA364-21:AC 300V 1 minute
Dielectric Withstanding Voltage	NO disruptive discharge.	EIA-364-20:Apply a voltageof 300VDC for 1 minute between adjacent terminals And between adjacent terminals and ground.

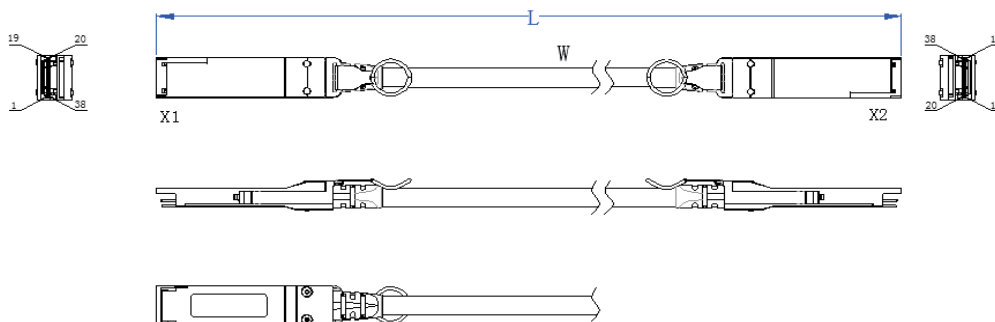
Environment Performance

ITEM	REQUIREMENT	TEST CONDITION
Operating Temp. Range	0°C to +70°C	Cable operating temperature range.
Storage Temp. Range (in packed condition)	-40°C to +80°C	Cable storage temperature range in packed condition.
Thermal Cycling Non-Powered	No evidence of physical damage	EIA-364-32D, Method A, -25 to 90C, 100 cycles, 15 min. dwells
Salt Spraying	48 hours salt spraying after shell corrosive area less than 5%.	EIA-364-26
Mixed Flowing Gas	Pass electrical tests per 3.1 after stressing. (For connector only)	EIA-364-35 Class II, 14 days.
Temp. Life	No evidence of physical damage	EIA-364-17C w/ RH, Damp heat 90°C at 85% RH for 500 hours then return to ambient
Cable Cold Bend	4H, No evidence of physical damage	Condition: -20°C ±2°C , mandrel diameter is 6 times the cable diameter.

Mechanical and Physical Characteristics

ITEM	REQUIREMENT	TEST CONDITION
Vibration	Pass electrical tests per 3.1 after stressing.	Clamp & vibrate per EIA-364-28E,TC-VII, test condition letter – D, 15 minutes in X, Y & Z axis.
Cable Flex	No evidence of physical damage	Flex cable 180° for 20 cycles ($\pm 90^\circ$ from nominal position) at 12 cycles per minute with a 1.0kg load applied to the cable jacket. Flex in the boot area 90° in each direction from vertical. Per EIA-364-41C
Cable Plug Retention in Cage	90N Min. No evidence of physical damage	Pull on cable jacket approximately 1 ft behind cable plug. No functional damage to cable plug below 90N. Per SFF-8432 Rev 5.0
Cable Retention in Plug	90N Min. No evidence of physical damage	Cable plug is fixtured with the bulk cable hanging vertically. A 90N axial load is applied (gradually) to the cable jacket and held for 1 minute. Per EIA-364-38B
Mechanical Shock	Pass electrical tests Per 3.1 after stressing.	Clamp and shock per EIA-364-27B, TC-G,3 times in 6 directions, 100g, 6ms.
Cable Plug Insertion	40N Max.	Per SFF-8436 Rev 5.4.1.
Cable plug Extraction	30N Max.	Place axial load on de-latch to de-latch plug. Per SFF-8436 Rev 5.4.1.
Durability	50 cycles, No evidence of physical damage	EIA-364-09, perform plug & unplug cycles: Plug and receptacle mate rate: 250times/hour. 50times for module (CONNECTOR TO PCB)

Mechanical Specifications

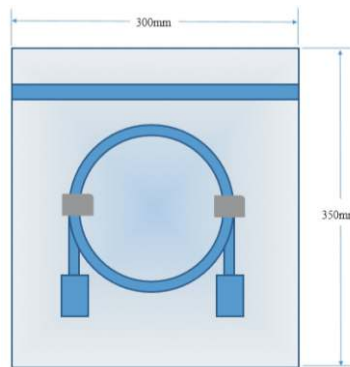


Wiring Diagram

X1	X2	REMARKS	X1	X2	REMARKS
18(RX1-)	37(TX1-)	pair	37(TX1-)	18(RX1-)	pair
17(RX1+)	36(TX1+)		36(TX1+)	17(RX1+)	
15(RX3-)	34(TX3-)	pair	34(TX3-)	15(RX3-)	pair
14(RX3+)	33(TX3+)		33(TX3+)	14(RX3+)	
6 (TX4+)	25(RX4+)	pair	25(RX4+)	6 (TX4+)	pair
5 (TX4-)	24(RX4-)		24(RX4-)	5 (TX4-)	
3 (TX2+)	22(RX2+)	pair	22(RX2+)	3 (TX2+)	pair
2 (TX2-)	21 (RX2-)		21 (RX2-)	2 (TX2-)	
1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	GND	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	EEPROM point at both ends

Package diagram

- <=2m: 200mm*300mm
- >2m: 300mm*350mm



Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
Version1.0	Tangzhiqiang	Li Tao	Ding zheng	New Released.	Nov 19, 2019



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